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White Paper

NEXT-GENERATION INTERFACES IN INDUSTRIAL LCD APPLICATIONS

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INTRODUCTION

For the past 15 years, application processors and industrial LCDs have been largely interface-compatible. In general, there have been two interfaces in industrial applications: digital RGB and LVDS. Most displays with resolutions VGA and below have been digital RGB while LVDS has become the de facto standard for resolutions WVGA and above. Embedded SOC devices will typically support one or the other of these two interfaces. As well, most single-board computers initially supported digital RGB and added LVDS as this interface gained in popularity.

LVDS has been used as an effective method to reduce radiated emissions in applications where the clock rates associated with higher-resolution displays can be problematic. For this reason, LVDS has become the more dominant interface as display resolutions continue to increase.

As additional applications have developed in the consumer market, we are starting to see a departure from the traditional industrial LCD interfaces. Namely, Embedded DisplayPort (eDP) and the Mobile Industry Processor Interface (MIPI®) Display Serial Interface (DSI) are starting to make their way into chipsets that are targeted at industrial applications. While Vx1 is emerging as the de facto standard for hi-res signage applications, eDP is the next-generation LCD interface coming out of the PC/notebook/tablet markets and MIPI DSI is the next-generation interface used in the handheld/smart phone markets. Chipsets targeted at either of these markets will support the appropriate interface. There are displays with these interfaces available in the market today; however, they are tied to the consumer markets and thus don't support the long-term life cycles generally required by traditional industrial applications.

At this time, the vast majority of industrial displays are LVDS-based and likely to remain that way for the foreseeable future. This document will discuss the new standards and silicon-based solutions that exist to bridge the interface gap from these standards to the traditional LVDS-based industrial LCDs. Vx1 solutions will also be explored and discussed.

THE eDP INTERFACE

In the PC market, the standard VGA and DVI interfaces are to be phased out over the next few years. VESA standard eDP will replace them and is now integrated into all mainstream GPUs and integrated GPU chip sets. As well, the Intel Bay Trail series of SOCs will support only the eDP interface going forward. This series consists of Intel Atom™ for tablets and 2-in-1 devices and Intel Pentium™ for entry 2-in-1 devices, laptops, desktops, and All-in-One PCs. Below are a few of the advantages of the eDP interface:

- Increased display performance
- Resolution (up to 4k × 2k at 60 FPS and 24 bpp)
- Refresh rate (up to 240 FPS for 1080p at 24 bpp)
- Color depth (up to 48 bpp at 2560 × 1600 at 60 FPS)
- Color accuracy (provides in-band color profile data)

- Multiple display support (up to 63 separate A/V streams are supported)
- Power reduction, increased battery life
- Cable consolidation
- Scalable for large and small devices, displays, and cables
- Single-lane (twisted pair) can support 1680 × 1050 at 18 bpp
- Easier chip integration, simpler physical interface
- Leads to lower system cost, lower power, and sleeker designs

Unlike other uncompressed data display interfaces, the data packet utilization is similar to communication standards such as Ethernet, USB, or SATA. It is a scalable interface and is future extensible to address new applications and system topologies. eDP uses a layered protocol for Isochronous AV Stream Transport: Stream and Link Policy Layers sit on top of Link (protocol) and Transport Layers, which reside on a Physical Layer. The Physical Layer is similar to LVDS in that it is a low-voltage, AC-coupled differential signal with default amplitude of 400 mV p-p. Up to four main links can be utilized and each main link uses 8B/10B encoding which provides an embedded clock and uses a pseudo random code for EMI mitigation. One of three fixed rates can be selected: 1.62 Gb/s, 2.7 Gb/s, or 5.4 Gb/s (eDP 1.2). Main link configurations are 1 lane, 2 lanes, or 4 lanes. The configuration needed is dependent on the display support required. In addition to the main data links, a bi-directional auxiliary channel and a Hot Plug Detect channel are incorporated in the standard interface. The interface is shown on the next page, in Figure 1.

eDP TO LVDS INTERFACE SOLUTIONS

There are several chip-level solutions available, as well as board-level products to facilitate various application needs. In general, these devices incorporate a Display-Port receiver and LVDS transmitter. They leverage eDP's source/sink "Link Training" routine to instantly bring up the video image once the initialization process is completed between the device and the system host. There is some variance among the solutions in terms of data rates, eDP version, and LVDS configuration, but they are all programmable to enable many configurations. The LVDS blocks also incorporate Spread Spectrum control to minimize radiated emissions. Backlight on/off and PWM con-
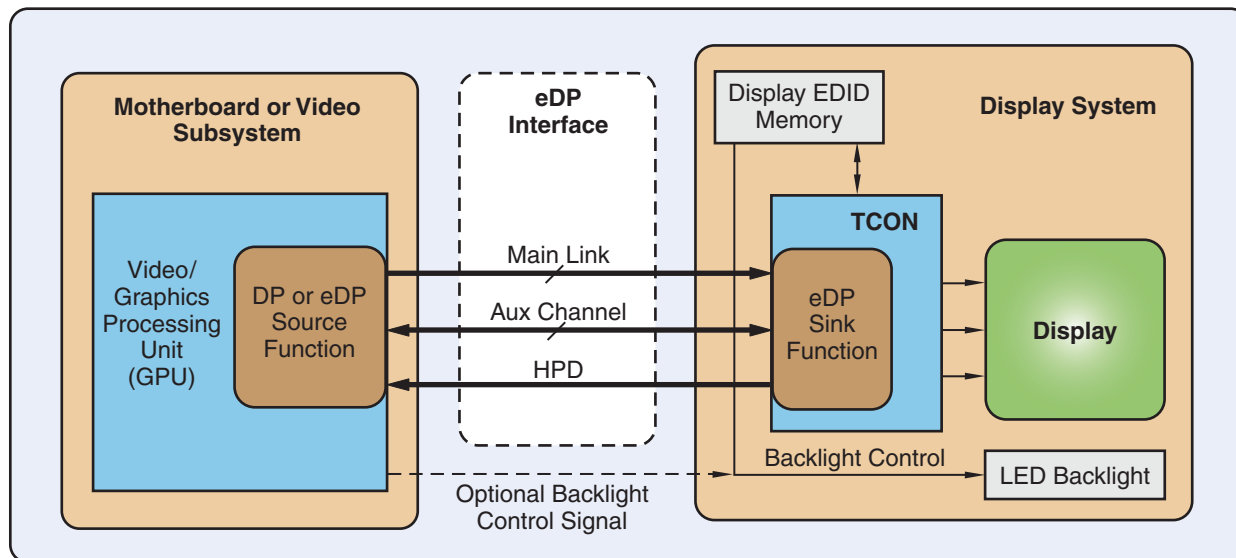
Figure 1. eDP Interface

trol functions are available and linked to brightness control commands sent through the AUX channel of the eDP link. Panel EDID and other configuration settings are typically loaded in a serial BOOT ROM connected to the conversion device. A summary of three options is shown below and detailed information can be found on the respective company's website.

Chrontel CH7511B

(www.chrontel.com)

- Supports eDP Specification version 1.2
- Supports 2 Main Link Lanes at 1.62 Gb/s or 2.7 Gb/s
- Supports 6/8-bit per pixel RGB format
- Supports Enhanced Framing Mode
- Supports VESA and CEA standard timing up to 1920 × 1200 resolution @ 60 Hz
- Supports 18-bit Single Port up to 24-bit Dual Port LVDS interface
- 68-pin QFN package

Analogix ANX1122

(www.analogix.com)

- Supports eDP Specification version 1.3
- Supports 2 Main Link Lanes at 1.62 Gb/s, 2.7 Gb/s, or 5.4 Gb/s

- Supports 6/8-bit per pixel RGB format
- Supports VESA and CEA standard timing up to 2560 × 1600 resolution @ 60 Hz
- Supports 18-bit Single Port up to 24-bit Dual Port LVDS interface
- 68-pin QFN package

NXP PTN3460

(www.nxp.com)

- Supports eDP Specification version 1.2
- Supports 2 Main Link Lanes at 1.62 Gb/s or 2.7 Gb/s
- Supports 6/8-bit per pixel RGB format
- Supports VESA and CEA standard timing up to 1920 × 1200 resolution @ 60 Hz
- Supports 18-bit Single Port up to 24-bit Dual Port LVDS interface up to 112 MHz pixel clock
- 56-pin QFN package

THE MIPI® DSI INTERFACE

As connectivity becomes more and more popular in industrial applications, the mobile chipsets will be utilized. Chipsets from Qualcomm, TI, and others all support the MIPI DSI interface. The MIPI Alliance is a consortium of over 275 member companies from the mobile market space.

MIPI DSI was also developed to simplify and cost-reduce the display interface in mobile devices. It defines a serial bus and a communication protocol between the host and the display device. At the physical layer, high-speed differential signaling is used, similar to both eDP and LVDS. The interface uses one high-speed clock lane and one or more data lanes. All the lanes travel from the host to the device, except lane 0, which can implement a bus turnaround (BTA) operation that allows it to change transmission direction. The interface has two modes of operation: low-power (LP) or high-speed (HS). In low-power mode, the high-speed clock is disabled and signal clocking information is embedded in the data. This mode is used for sending configuration information and commands. High-speed mode enables the high-speed clock lane for transmitting image data.

The communication protocol uses two sets of instructions. The Display Command Set (DCS) is a set of common commands used to control the display device and the format of these commands is specified by the DSI standard. Part of this definition includes registers that can be addressed and their operation. Basic commands like Sleep, Enable, and Invert Display are included. The Manufacturer Command Set (MCS) is a command space that is device specific and often includes commands required to program non-volatile memory, set gamma correction values, or other actions not described in the DSI standard. Data packets are defined in the standard and include a Data ID, word count, Error Correction Code (ECC), Payload, and Checksum (CRC). Horizontal and Vertical blanking information is interleaved with the image data on the lanes. The data is sent in real time and not stored by the device, which allows for simpler display configurations without frame buffer memory. A typical refresh rate of 60 FPS must be utilized to maintain the image. An interface overview is shown on the next page, in Figure 2.

MIPI DSI TO LVDS INTERFACE SOLUTIONS

Again, there are several chip-level solutions in the market that enable a DSI to LVDS Bridge. These devices implement the MIPI D-PHY front-end and some version of the DSI standard definition. The devices decode the DSI data packets and convert the formatted video data to a LVDS output stream. They can include partial line buffering to accommodate any data stream mismatch between the DSI and LVDS interface. They also typically include a I^2C bus

for device initialization and configuration. A summary of two options is shown below and detailed information can be found on the respective company's URL listed.

Texas Instruments SN76DSI85

(www.ti.com)

- Implements MIPI® D-PHY Version 1.00.00 and DSI Version 1.02.00
- Single Channel DSI Receiver configurable for one, two, three, or four Data Lanes, and one Clock Lane
- Supports 18 bpp and 24 bpp DSI Video Packets
- Supports up to 1920 × 1200 resolution @ 60 Hz and 24 bpp Color
- Supports Single and Dual Port LVDS interfaces with a max clock rate of 154 MHz
- Low-power features including Shutdown, Reduced LVDS Voltage Swing, and MIPI ULPS Support
- I^2C port for initialization
- 68-pin BGA (ZQE) package

Toshiba TC358765

(www.toshiba.com/taec)

- Implements MIPI D-PHY Version 0.9 and DSI Version 1.01
- Single Channel DSI Receiver configurable for one, two, three, or four Data Lanes, and one Clock Lane
- Supports 18bpp and 24bpp DSI Video Packets
- Supports up to 1920 × 1200 resolution @ 60 Hz and 18 bpp Color
- Supports Single and Dual Port LVDS interfaces with a max clock rate of 85 MHz
- Utilizes the Toshiba proprietary Magic Square algorithm to interpolate RGB666 to pseudo RGB888 image data
- I^2C port for initialization
- 64-pin P-TFBGA package

THE Vx1 INTERFACE

LVDS has been the go-to standard for Industrial LCD applications above VGA resolution. However, as large-area displays have moved from HD to FHD resolution and beyond, the need for a more robust interface has arisen. Vx1 is a similar signaling standard but can run at faster speeds over inexpensive twisted-pair copper cables.

Developed by Thine Electronics in 2007, its Equalizer and CDR technologies enable speeds of 840 MB/s for each
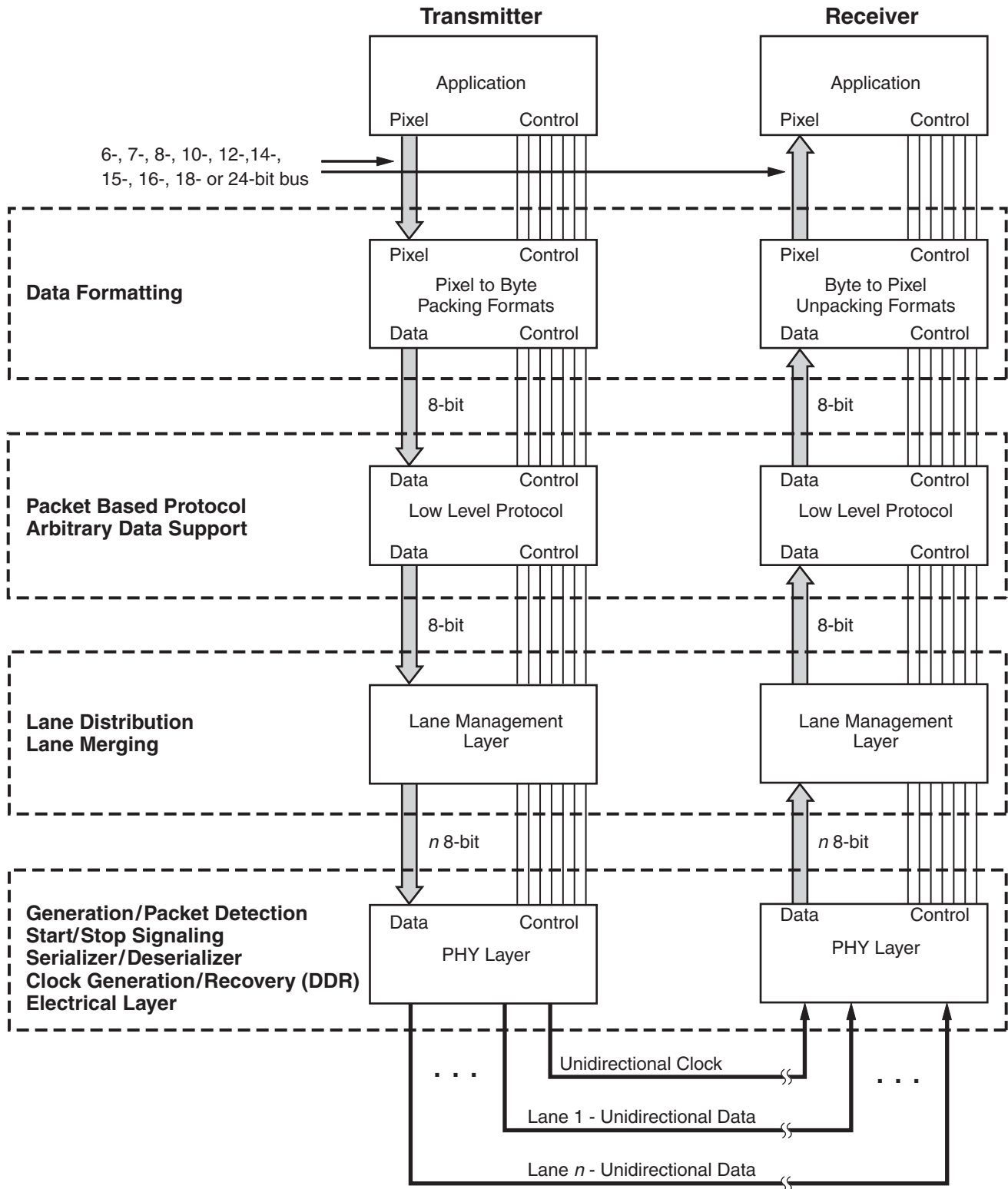
Figure 2. MIPI DSI Interface

twisted-pair. Subsequently, the Vx1 HS extension increases the bandwidth to 3.75 Gbit/s for each twisted-pair. This helps to reduce cabling cost and helps to minimize skew issues, EMI, and power consumption. The system is also somewhat cable agnostic in that any LAN, SATA, HDMI, Display Port, etc. cable can be used as long as it is an impedance-matched 100 Ω cable. The equalizer portion enables higher data rates over longer cable lengths; the initial Vx1 standard supports 10 M cable lengths. The CDR (Clock Data Recovery) function solves the skew issues that are more prevalent in LVDS as the resolutions and color depths continue to increase. CDR eliminates a separate clock pair and embeds the clock within the image data

stream. Since there is no fixed frequency clock pair, emissions are lowered and wire counts are reduced.

For example, a FHD screen with 10-bit color depth and double frame rate requires 24 pairs of LVDS cabling. In this case skews need to be in the several hundred picoseconds range because of the high-speed clock and data rate. In addition, because LVDS uses signaling between zero and 1.2 V, it is more difficult to design LSI circuits using lower-voltage high-density processes. This same example would only require two twisted pairs when implemented using Vx1. An overview is shown in Figure 3.
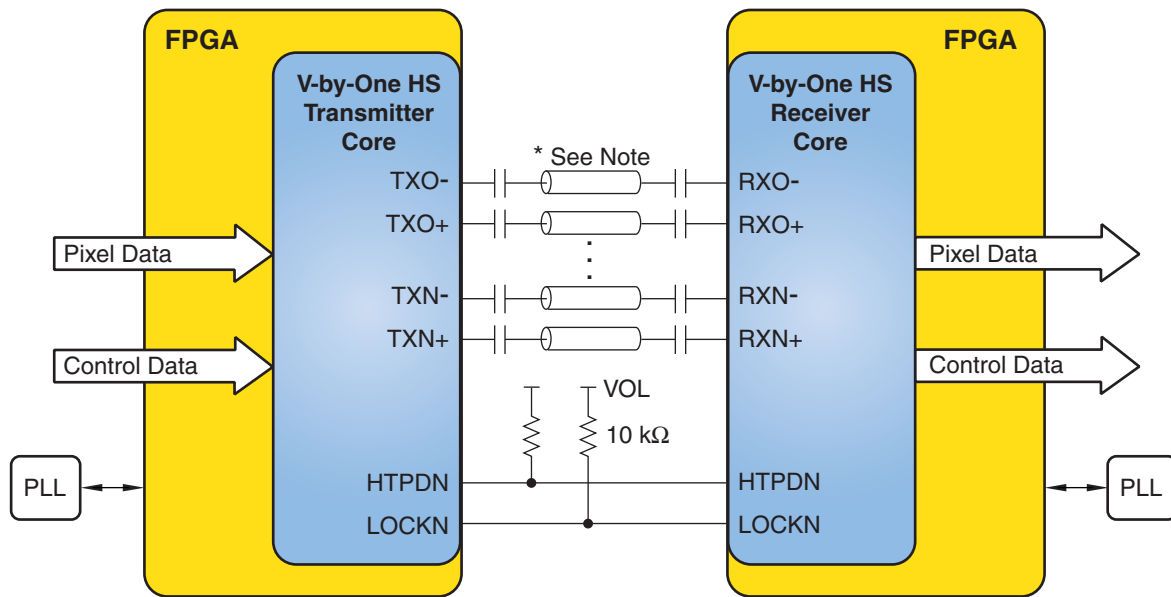
Figure 3. Vx1 Interface

Vx1 enables transmission of up to 40-bit video data, 24-bit CTL data, HSYNC, VSYNC, and DE by twisted pair cabling. In addition, the link includes Hot Plug Detect and CDR Lock signals. The number of data lanes is based on the resolution and color depth as shown in Table 1:

VX1 INTERFACE SOLUTIONS

Thine:
(http://www.thine.co.jp/en/products/lineup/)

The original Vx1 chipset from Thine consists of a THCV213 transmitter and THCV214 receiver. This initial chipset supports a 5 – 40 MHz pixel clock, 18-bit data, 3-bit Sync signals, and two Vx1 data lane outputs. Both parts use a 3.3V supply and a TQFP48 package. This enables a low-cost, simple cable solution for SVGA and below. Dash numbers for industrial temp
(0 to 70°C) and automotive temp (-40°C to 85°C) are available.

Initial Vx1 HS chipsets from Thine were the THCV217

Table 1. Vx1 Parameters

Resolution	Refresh Rate (Pixel Clock)	Color Depth	# of Lanes
HD: 1280 × 720	60 Hz (74.25 MHz)	Up to 36-bit	1
	120 Hz (148.5 MHz)	Up to 36-bit	2
	240 Hz (297 MHz)	Up to 36-bit	4
Full HD: 1920 × 1080	60 Hz (148.5 MHz)	Up to 36-bit	2
	120 Hz (297 MHz)	Up to 36-bit	4
	240 Hz (594 MHz)	Up to 36-bit	8
	480 Hz (1188 MHz)	Up to 36-bit	16
Cinema - Full HD: 2560 × 1080	60 Hz (185 MHz)	Up to 30-bit	2
	120 Hz (370 MHz)	Up to 30-bit	4
	240 Hz (740 MHz)	Up to 30-bit	8
4K × 2K: 3840 × 2160	60 Hz (594 MHz)	Up to 36-bit	8
	120 Hz (1188 MHz)	Up to 36-bit	16
	240 Hz (2376 MHz)	Up to 36-bit	32

transmitter and THCV218 receiver. This chipset supports 2 LVCMOS input ports at 32-bits/pixel and 2 Vx1 HS output lanes, enabling 2.72 Gbps data rates. Depending on configuration, the transmitter can support pixel clocks up to 170 MHz with 32-bit data, for up to 1080p/60 Hz/30-bit color. They support both 1.8V and 3.3V supplies and the 217 is in a TFBGA105 package, while the 218 is in a TFBGA145 package. Both parts are rated -20°C to 85°C.

Also available from Thine are chipsets that convert from standard LVDS to Vx1 HS and back. The THCV215 transmitter supports 6ch LVDS 2-port (Dual Pixel Link) input at 36-bits/pixel and 140-700 Mbps/ch. It runs at 1.8V or 3.3V and is in a TSSOP64 package. It can be used with either the THCV216 or THCV218 receiver. In addition, the THCV226 receiver supports 4 pairs of Vx1 HS lanes. This enables video data transmission of up to 1080p/10-bit color/120 Hz refresh. The max data rate is 3.4 Gbps/lane. It supports a 1.8 V supply and is in a TQFP128 package.

Altera:

(https://www.altera.com/solutions/technology/transceiver/protocols/pro-v-by-one.html)

Altera has multiple FPGA solutions that can be used to implement Vx1 HS lanes at up to 3.75 Gbps data rates. These include: Cyclone IV GX, Arria V, Arria II GX, and Stratix IV GX FPGAs. They include support for 1 to 32 lanes, user-selectable color depth from 18 to 32-bits, automatically capture/convert refresh rate to pixel clock speed (i.e. 60 Hz @

74.25 MHz) and are compatible with Altera's Video and Image Processing (VIP) IP Suite. The solutions combine the Vx1 HS IP core, FPGA development hardware and embedded transceiver I/O to support the physical layers of the Vx1 HS protocol.

Digital View:

(http://www.digitalview.com/products/svx-3840-lcd-controller)

The SVX-3840 is a board-level solution that provides:

- Up to 4K input with connectivity to 60/120 Hz 4K panels
- Support for 4K (3840 × 2160), 60/120 Hz, 10-bit color
- Support for 8 and 16 lane Vx1 HS
- HDMI 1.4, DP 1.2, DVI, and ARGB inputs
- Programmable hot-keys
- OSD Menu transparency
- Picture-in-Picture (PIP)
- Ethernet and RS-232 control

CONCLUSION

Embedded, industrial applications will start using system and SOC architectures that only support the next-gen interfaces used in the PC and mobile markets. The eDP and MIPI DSI interfaces have been discussed. These interfaces are not compatible with the standard LVDS interface used on the majority of long-lifecycle, industrial LCDs. Chip-level solutions to bridge these interface differences have been identified and summarized for use with the various system architectures. In addition, the Vx1 interface has been discussed, along with chip-level and board-level interface solutions. Vx1 is emerging as the go-to interface for large-area, high-resolution displays used in corporate AV and digital signage applications. Additional application details can be found on the respective company websites.

All web links to non-Sharp companies were operational and relevant at date of publication.

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